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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER	
YUEN, KAN	
ART UNIT	**PAPER NUMBER**
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/766,282	GUNTURI ET AL.	
	Examiner	Art Unit	
	Kan Yuen	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Specification

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
    (1) Field of the Invention.
    (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Objections

1. Claims 5,6,9,14,18 are objected to because of the following informalities:

In claim 5, line 2, the term "and" should be changed to "or", because it only claimed one. Similar problem exist in claims 6, 9, 14, and 18.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-5, 7, 8, 10-14, 16, 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Calvignac et al. (Pat No.: 7167471).

In claim 1, Calvignac et al. disclosed the method of registering, in response to an instruction included in source code for an upstream component, a procedure at a downstream component in a packet processing pipeline, the procedure being associated with at least one event (see column 5, lines 47-60, and see fig. 1-2). In fig. 2, the packet processor 103 comprises a pipeline processing unit: processor 201, tree search engine 202 and DS memory 206, where processor 201 can be considered as the upstream component, and register 212 in the unit tree search engine 202 can be the downstream component. The register 212 may be configured to register definitions associated with various tables. Therefore we can interpret that the definition is the

procedure and the various tables are the associated event. Because processor 201 needs to communicate with CAM 211 through the tree search engine 202 unit, to determine whether CAM 211 is required to identify the data structure in the DS memory 206, therefore in response to this, register 212 must register the table definition for further data processing; processing a received packet at the upstream component executing on a first engine; processing the packet at the downstream component executing on a second engine after the processing of the received packet at the upstream component, the processing at the downstream component comprising: determining occurrence of the at least one associated event at the downstream component; and in response, executing the registered procedure at the second engine (see column 4, lines 56-67, and see column 5, lines 35-60). As the processor 201 received a packet, it processed the packet by generate a search key from the header of the packet, where generation in the processor 201 is the first engine. Then the data is forwarded to the register 212 where the register stores the packet definition, and the storing can be the second engine. If the table definition or the occurrence event indicates to search the table using CAM211, then processor 201 may be configured to transfer or executing the key to register the key to register 213 or the second engine.

Regarding claim 2, Calvignac et al. disclosed the method of the first engine and second engine comprise engines integrated on the same semiconductor die (see column 4, lines 5-20, and see fig. 2). The first engine or processor 201 and the second engine or register 212, are in the packet processor unit 103, or the same semiconductor die.

Regarding claim 3, Calvignac et al. disclosed the method of the first engine and the second engine comprise multi-threaded engines (see column 4, lines 5-20, and see fig. 2). Processor 201 and register 212 are two separate engines therefore they are multi-threaded engines.

Regarding claim 4, Calvignac et al. disclosed the method of the procedure comprises a procedure that alters data structures defined by the upstream component (see column 5, lines 45-60). The table definition or procedure stored in the register 212 may be used to triggers the CAM 211 to search the table to identify the data structure in 206 associated with the received packet from the processor 201.

Regarding claim 5, Calvignac et al. disclosed the method of the upstream component and downstream component comprise one of: adjacent components in the pipeline and non-adjacent components in the pipeline (see column 4, lines 5-20, and see fig. 2). The processor 201 and register 212 are located adjacent to each other.

Regarding claim 7, Calvignac et al. disclosed the method of the registering comprises loading instructions for the procedure into the second engine (see column 4, lines 56-67, and see fig. 2). The register 212 may be configured to store table definition, where the definition has the access or instruction to communicate with the CAM 211.

Regarding claim8, Calvignac et al. disclosed the method of the registering comprises registering the procedure with an event handler that invokes registered procedures in response to events signaled by the downstream component (see column 5, lines 45-60). The table definition or procedure stored in the register 212 may be used

to triggers or invoke the CAM 211 to search the table to identify the data structure in 206 associated with the received packet from the processor 201.

Regarding claim 10, Calvignac et al. disclosed the method of access instructions of an upstream component in a packet processing pipeline, the upstream component to be executed by a first engine (see column 4, lines 56-67, and see column 5, lines 47-60, and see fig. 1-2). In fig. 2, the packet processor 103 comprises a pipeline processing unit: processor 201, tree search engine 202 and DS memory 206, where processor 201 can be considered as the upstream component, and register 212 in the unit tree search engine 202 can be the downstream component. As the processor 201 received a packet, it processed the packet by extracting one or more fields from the packet header in the received packet and generates a search key, where generation in the processor 201 is the first engine. Where the key is used to access various table or instruction; register, in response to an accessed instruction of the upstream component, a procedure at a downstream component in the packet processing pipeline to be executed by a second engine, the procedure to be executed on the second engine in response to the downstream component detecting the occurrence of at least one event (see column 4, lines 56-67, and see column 5, lines 35-60). The data is forwarded to the register 212 where the register stores the packet definition, and the storing can be the second engine. If the table definition or the occurrence event indicates to search or detect the table using CAM211, then processor 201 may be configured to transfer or executing the key to register the key to register 213 or the second engine.

Regarding claim 11, Calvignac et al. disclosed the method of the first engine and second engine comprise engines integrated on the same semiconductor die (see column 4, lines 5-20, and see fig. 2). The first engine or processor 201 and the second engine or register 212, are in the packet processor unit 103, or the same semiconductor die.

Regarding claim 12, Calvignac et al. disclosed the method of the first engine and the second engine comprise multi-threaded engines (see column 4, lines 5-20, and see fig. 2). Processor 201 and register 212 are two separate engines therefore they are multi-threaded engines.

Regarding claim 13, Calvignac et al. disclosed the method of the procedure comprises a procedure that alters data structures defined by the upstream component (see column 5, lines 45-60). The table definition or procedure stored in the register 212 may be used to triggers the CAM 211 to search the table to identify the data structure in 206 associated with the received packet from the processor 201.

Regarding claim 14, Calvignac et al. disclosed the method of the upstream component and downstream component comprise one of: adjacent components in the pipeline and non-adjacent components in the pipeline (see column 4, lines 5-20, and see fig. 2). The processor 201 and register 212 are located adjacent to each other.

Regarding claim 16, Calvignac et al. disclosed the method of the instructions to register comprise instructions to load instructions for the procedure into the second engine (see column 4, lines 56-67, and see fig. 2). The register 212 may be configured

to store table definition, where the definition has the access or instruction to communicate with the CAM 211.

Regarding claim 17, Calvignac et al. disclosed the method of the instructions to register comprises instructions to register the procedure with an event handler that invokes registered procedures in response to events signaled by the downstream component (see column 5, lines 45-60). The table definition or procedure stored in the register 212 may be used to triggers or invoke the CAM 211 to search the table to identify the data structure in 206 associated with the received packet from the processor 201.

Claim Rejections - 35 USC § 103

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 6, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calvignac et al. (Pat No.: 7167471), in view of Johnson et al. (Pat No.: 6920146).

For claim 6, Calvignac et al. disclosed all the subject matter of the claimed invention with the exception of the registering comprises one of: run-time registering and compile-time registering. Johnson et al. from the same or similar fields of endeavor teach the method of the registering comprises one of: run-time registering and compile-time registering (see paragraph 0040, lines 1-6). The Dbus is allowed to monitor the register at run-time or compile-time. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the method as taught by Johnson et al. in the network of Calvignac et al. The motivation for using the method as taught by Johnson et al. in the network of Calvignac et al. being that the system increases the speed of registering.

Regarding claim 15, Johnson et al. disclosed a compiler (see paragraph 0040, lines 1-6). The Dbus is allowed to monitor the register at run-time or compile-time.

8. Claims 9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calvignac et al. (Pat No.: 7167471), in view of Drort et al. (Pub No.: 2003/0193953).

For claim 9, Calvignac et al. disclosed all the subject matter of the claimed invention with the exception of the packet processing pipeline comprises one of the following: an IPv4 packet processing pipeline, an IPv6 packet processing pipeline, and an Asynchronous Transfer Mode (ATM) packet processing pipeline. Drort et al. from the same or similar fields of endeavor teaches the method of the packet processing pipeline comprises one of the following: an IPv4 packet processing pipeline, an IPv6 packet processing pipeline, and an Asynchronous Transfer Mode (ATM) packet processing pipeline (see paragraph 0026, lines 10-25). Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the method as taught by Drort et al. in the network of Calvignac et al. The motivation for using the method as taught by Drort et al. in the network of Calvignac et al. being that the system will improve the system resources such as bandwidth availability.

Regarding claim 18, Drort et al. disclosed the method of the packet processing pipeline comprises one of the following: an IPv4 packet processing pipeline, an IPv6 packet processing pipeline, and an Asynchronous Transfer Mode (ATM) packet processing pipeline (see paragraph 0026, lines 10-25).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Matsuoka et al. (Pat No.: 6920145), Comeau et al. (Pub No.: 2001/0049726), and Schwartz et al. (Pat No.: 6804241), are show systems which considered pertinent to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kan Yuen whose telephone number is 571-270-2413. The examiner can normally be reached on Monday-Friday 10:00a.m-3:00p.m EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky O. Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ky

RICKY O. NGO
SUPERVISORY PATENT EXAMINER